AMENDMENTS TO CLAIMS

The following listing of the claims replaces all prior claim versions and listings.

1. (Previously Presented) A memory access control device comprising:

a memory master to request access to memory;

a memory control unit to produce control signals of memories based on access information to be output from said memory master; and

a hit predicting unit to predict whether or not a next access to each bank in memory will be directed to a same page;

wherein, when a hit predicting unit predicts a hit, said memory control unit terminates a routine without closing a bank at a time of completion of present access operations and, when said hit predicting unit predicts a miss, said memory control unit closes said bank at the time of completion of present access operations and terminates the routine.

2. (Previously Presented) The memory access control device according to claim 1, wherein, for each of a last "n" (n is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss has been found, and said hit predicting unit predicts a hit, if a number of times of accesses out of the last "n" times of accesses is "m" or more ($m \leq n$: "m"is a natural number), and said hit predicting unit predicts a miss, if said number of times of accesses is not "m" or more.

3. (Previously Presented) The memory access control device according to claim 1, wherein,for each of a last "j" ("j" is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss has been found, and said hit predicting unit predicts a hit when a hit has been found in all of the last "j" times of

accesses, and said hit predicting unit predicts a miss if no hit has been found at least one time in all of the last "j" times of accesses.

4. (Previously Presented) The memory access control device according to claim 1, wherein, for each of a last "k" ("k" is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss has been found, and said hit predicting unit predicts a miss if a miss has been found in all of the last "k" times of accesses, and said hit predicting unit predicts a hit, if a hit has been found at least one time in all of the last "k" times of accesses.

5. (Previously Presented) The memory access control device according to claim 1, wherein, for each of a last "n" ("n" is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss has been found, and said hit predicting unit predicts a miss when a miss has been found in all of the last "k" times of accesses ($k \leq n$: "k" is a natural number) out of the last "n" times of accesses, and said hit predicting unit predicts a hit when a hit has been found at least one time in all of the last "k" times of accesses out of the last "n" times of accesses and if a hit has been found in all of the last "j" times of accesses ($j \leq n$: "j" is a natural number) out of the last "n" times of accesses, and said hit predicting unit predicts a hit when a miss has been found at least one time in all of the last "j" times of accesses out of the last "n" times of accesses, and if a number of times of accesses by which a hit has been found out of the last "n" times of accesses is "m" times or more ($m \leq n$: "m" is a natural number), and said hit predicting unit predicts a miss when a number of times of accesses by which a hit has been found out of the last "n" times of accesses is not "m" times or more.

6. (Previously Presented) The memory access control device according to claim 1,

wherein after a bank and a page to be accessed next have been determined, said memory master informs said memory control unit of information about said bank and said page to be accessed and wherein said memory control unit, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is the page being presently accessed, said memory control unit terminates the routine, regardless of the prediction from said hit predicting unit, without closing said bank being presently accessed at the time of completion of present access operations and, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and the memory control unit terminates the routine.

7. (Previously Presented) The memory access control device according to claim 2, wherein after a bank and a page to be accessed next have been determined, said memory master informs said memory control unit of information about said bank and said page to be accessed and wherein said memory control unit, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is the page being presently accessed, said memory control unit terminates the routine, regardless of the prediction from said hit predicting unit, without closing said bank being presently accessed at the time of completion of present access operations and, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is different from

the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and said memory control unit terminates the routine.

8. (Previously Presented) The memory access control device according to claim 3, wherein after a bank and a page to be accessed next have been determined, said memory master informs said memory control unit of information about said bank and said page to be accessed and wherein said memory control unit, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is the page being presently accessed, said memory control unit terminates the routine, regardless of the prediction from said hit predicting unit, without closing said bank being presently accessed at the time of completion of present access operations and, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and said memory control unit terminates the routine.

9. (Previously Presented) The memory access control device according to claim 4, wherein after a bank and a page to be accessed next have been determined, said memory master informs said memory control unit of information about said bank and said page to be accessed and wherein said memory control unit, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by

said memory master is the page being presently accessed, said memory control unit terminates the routine, regardless of the prediction from said hit predicting unit, without closing said bank being presently accessed at the time of completion of present access operations and, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and said memory control unit terminates the routine.

10. (Previously Presented) The memory access control device according to claim 5, wherein after a bank and a page to be accessed next have been determined, said memory master informs said memory control unit of information about said bank and said page to be accessed and wherein said memory control unit, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is the page being presently accessed, said memory control unit terminates the routine, regardless of the prediction from said hit predicting unit, without closing said bank being presently accessed at the time of completion of present access operations and, if said bank to be accessed next by said memory master is the bank being presently accessed and said page to be accessed by said memory master is different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and said memory control unit terminates the routine.

11. (Previously Presented) A memory access control device comprising:

two or more memory masters to request access to memory; an arbiter unit to arbitrate memory access requests fed from said memory masters and to select access information fed from any one of said memory masters;

a memory control unit to produce a control signal of memory based on access information output from said arbiter unit; and

a hit predicting unit to predict whether or not a next access to each bank in memory will be directed to a same page;

wherein, when said hit predicting unit predicts a hit, said memory control unit terminates a routine without closing said bank at a time of completion of present access operations, and when said hit predicting unit predicts a miss, said memory control unit closes said bank at the time of present access operations and terminates the routine.

12. (Currently Amended) The memory access control ~~unit~~ device according to claim 11, wherein, for each of a last "n" ("n" is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss hit has been found and said hit predicting unit predicts a hit, if a number of times of accesses out of the last "n" times of accesses is "m" or more ($m \leq n$: "m" and "n" each is a natural number), and said hit predicting unit predicts a miss, if said number of times of accesses is not "m" or more.

13. (Previously Presented) The memory access control device according to claim 11, wherein, for each of a last "j" ("j" is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss has been found, and said hit predicting unit predicts a hit when a hit has been found in all of the last "j" times of

accesses, and said hit predicting unit predicts a miss if no hit has been found in all of the last "j" times of accesses.

14. (Previously Presented) The memory access control device according to claim 11, wherein, for each of a last "k" ("k" is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss has been found, and said hit predicting unit predicts a miss if a miss has been found in all of the last "k" times of accesses, and said hit predicting unit predicts a hit if a hit has been found in all of the last "k" times of accesses.

15. (Previously Presented) The memory access control device according to claim 11, wherein, for each of a last "n" ("n" is a natural number) times of accesses to each bank in memory, said hit predicting unit stores whether a hit or a miss has been found, and said hit predicting unit predicts a miss when a miss has been found in all of the last "k" ($k \leq n$: "k" is a natural number) times of accesses out of the last "n" times of accesses, and said hit predicting unit predicts a hit when a hit has been found at least one time in all of the last "k" times of accesses out of the last "n" times of accesses and if a hit is found in all of the last "j" times of accesses ($j \leq n$: "j" is a natural number) out of the last "n" times of accesses, and said hit predicting unit predicts a hit when a miss has been found at least one time in all of the last "j" times of accesses out of the last "n" times of accesses, and if a number of times of accesses by which a hit has been found out of the last "n" times of accesses is "m" times or more ($m \leq n$: "m" is a natural number), and said hit prediction unit predicts a miss, when a number of times of accesses by which a hit has been found out of the last "n" times of accesses is not "m" times or more.

16. (Previously Presented) The memory access control device according to claim

11, wherein after a bank and a page to be accessed next have been determined, each memory master informs said arbiter unit and said memory control unit of information about said bank and said page to be accessed next and wherein said memory control unit, if there exists said memory master which gets the next access to the bank being presently accessed and to the page being presently accessed, said memory control unit terminates the routine without closing said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and, if there exists said memory master which gets the next access to the bank being presently accessed and to a page different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from the hit predicting unit, and said memory control unit terminates the routine, and if there exists said memory master which gets the next access to the bank being presently accessed and the page being presently accessed, said arbiter unit selects said memory master with priority.

17. (Previously Presented) The memory access control device according to claim 12, wherein after a bank and a page to be accessed next have been determined, each memory master informs said arbiter unit and said memory control unit of information about said bank and said page to be accessed next and wherein said memory control unit, if there exists said memory master which gets the next access to the bank being presently accessed and to the page being presently accessed, said memory control unit terminates the routine without closing said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and, if there exists said memory master which gets the next access to the bank being

presently accessed and to a page different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from the hit predicting unit, and said memory control unit terminates the routine, and if there exists said memory master which gets the next access to the bank being presently accessed and the page being presently accessed, said arbiter unit selects said memory master with priority.

18. (Previously Presented) The memory access control device according to claim 13, wherein after a bank and a page to be accessed next have been determined, each memory master informs said arbiter unit and said memory control unit of information about said bank and said page to be accessed next and wherein said memory control unit, if there exists said memory master which gets the next access to the bank being presently accessed and to the page being presently accessed, said memory control unit terminates the routine without closing said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and, if there exists said memory master which gets the next access to the bank being presently accessed and to a page different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from the hit predicting unit, and said memory control unit terminates the routine, and if there exists said memory master which gets the next access to the bank being presently accessed and the page being presently accessed, said arbiter unit selects said memory master with priority.

19. (Previously Presented) The memory access control device according to claim 14, wherein after a bank and a page to be accessed next have been determined, each

memory master informs said arbiter unit and said memory control unit of information about said bank and said page to be accessed next and wherein said memory control unit, if there exists said memory master which gets the next access to the bank being presently accessed and to the page being presently accessed, said memory control unit terminates the routine without closing said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and, if there exists said memory master which gets the next access to the bank being presently accessed and to a page different from the page being presently accessed, said memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from the hit predicting unit, and said memory control unit terminates the routine, and if there exists said memory master which gets the next access to the bank being presently accessed and the page being presently accessed, said arbiter unit selects said memory master with priority.

20. (Previously Presented) The memory access control device according to claim 15, wherein after a bank and a page to be accessed next have been determined, each memory master informs said arbiter unit and said memory control unit of information about said bank and said page to be accessed next and wherein said memory control unit, if there exists said memory master which gets the next access to the bank being presently accessed and to the page being presently accessed, said memory control unit terminates the routine without closing said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from said hit predicting unit, and, if there exists said memory master which gets the next access to the bank being presently accessed and to a page different from the page being presently accessed, said

memory control unit closes said bank being presently accessed at the time of completion of present access operations, regardless of the prediction from the hit predicting unit, and said memory control unit terminates the routine, and if there exists said memory master which gets the next access to the bank being presently accessed and the page being presently accessed, said arbiter unit selects said memory master with priority.